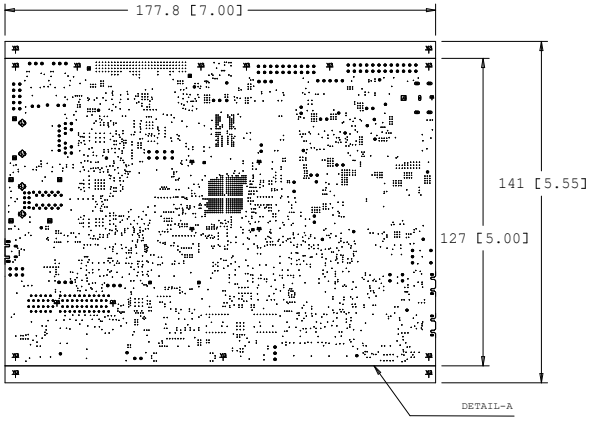
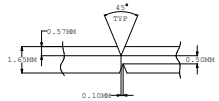
REVISIONS		
REV #	DESCRIPTION	DATE
REV #	CCN #	DDMMYY

FABRICATION NOTES:

1. FABRICATE PCB IN ACCORDANCE WITH IPC-6012D, CLASS 2; PER IPC-6011. PCB SHALL BE MANUFACTURED USING ITEQ IT 180A OR EQUIVALENT
2. MATERIALS:
   1. LAMINATE AND PREPREG (B-STAGE) TO BE IN ACCORDANCE WITH IPC-4101/126. (MIN.TG 170)
   2. COPPER FOIL TO BE IN ACCORDANCE WITH IPC-MF-150. UNLESS OTHERWISE SPECIFIED, ALL COPPER WEIGHT FOR INNER SIGNAL LAYERS AND INNER PLANE LAYERS TO BE 35UM (1 OZ.). FOR OUTER LAYERS 35UM (1 OZ). COPPER WEIGHT IS TO BE CONSIDERED "FINISHED". THE COPPER FOIL THICKNESS TOLERANCES SHALL BE AS PER IPC 6012B TABLE NO.3-7 AND 3-8.
3. ALL HOLES SHALL BE LOCATED WITHIN 0.13MM DIAMETER OF TRUE POSITION. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.125MM.
4. BOW AND TWIST SHALL NOT EXCEED MORE THAN 0.75% OF THE DESIGN LENGTH.
5. CONDUCTOR WIDTH SHALL NOT BE LESS THAN 20% FROM ITS ORIGINAL DATA. INCASE FOR MATCHING IMPEDANCE MISTRAL SHALL APPROVE THE MODIFIED WIDTHS AND SPACING. TRACE WIDTH SHALL BE MEASURED ON THE SURFACE IN CONTACT WITH THE LAMINATE.
6. BOARD FINISHED SHALL BE ACCORDING TO IPC-6012D CLASS 2.
7. AUTOMATED OPTICAL INSPECTION OF ALL THE LAYERS IS REQUIRED.
8. FINISH:
   1. ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDER MASK OR OTHER PLATING SHALL BE ENIG, ELECTROLESS NICKEL/IMMERSION GOLD, ELECTROLESS NICKEL SHALL BE 3-6 MICRONS, TYPICAL IMMERSION GOLD THICKNESS SHALL BE 0.04-0.06 MICRONS OF SOLDERABLE IMMERSION GOLD SURFACE.
   2. APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK PER IPC-SM-840, CLASS H, TO BOTH SIDES OF THE BOARD OVER BARE COPPER. VIA HOLES SHALL BE RESIN FILLED AND COVERED WITH SOLDER MASK. ONLY SOLDER MASK IMAGES THAT ARE 0.08(0.003") PER SIDE SHALL BE REDUCED IF REQUIRED. ALL OTHER SOLDER MASK IMAGES SHALL NOT BE ENLARGED. DEFAULT COLOUR OF SOLDER MASK SHALL BE GREEN.
   3. SILKSCREEN SHALL BE WHITE, PERMANENT, ORGANIC, NON-CONDUCTIVE INK. THERE SHALL BE NO SILKSCREEN ON ANY SOLDERABLE COMPONENT PAD. CLIPPING OF SILK SCREEN SHALL BE ALLOWED IF THE SILK SCREEN FALLS ON SOLDERABLE AREAS.
   4. SURFACE AND VIA HOLES FINISH SHALL NOT BE LESS THAN 200M [0.00079"], INCASE OF LASER VIA'S, BLIND VIA'S SHALL NOT BE LESS THAN 120M [0.00047"] AND BURIED VIA'S SHALL NOT BE LESS THAN 150M [0.0006"].
   5. ALL HOLES SURROUNDED BY LAND <=0.010" SHALL BE COMPLIANCE TO IPC6012, CLASS 2.
9. MARKING:
   1. BOARD SHALL MEET THE REQUIREMENTS OF UL-796E WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN SILKSCREEN.
10. TEST REQUIREMENTS:
    1. 100% NET LIST ELECTRICAL VERIFICATION USING MISTRAL SUPPLIED IPC-D-356 NET LIST FOR OPENS AND SHORTS.
11. THIEVING IS ALLOWED ONLY IN THE PANEL FRAME, NOT IN THE CIRCUIT AREA.
12. TEAR DROPS SHALL BE ADDED ON VIA'S AND THROUGH HOLE PADS IN ALL INTERNAL AND OUTER LAYERS.
13. ALL UNCONNECTED VIA'S SHALL BE SUPPRESSED IF REQUIRED.
14. FINISHED PCB THICKNESS SHALL BE 0.065" +/-10%.
15. MIN TRACE WIDTH/SPACING ON BOARD IS 0.0032"/0.0037".
16. ENSURE UL REGISTERED E-FILE NUMBER SHALL BE PRINTED ON THE PCB SILKSCREEN.
17. VIA ON PAD SHALL BE RESIN FILLED AND CAP-PLATED.
18. FOR STACKUP DETAIL PROC101_STACKUP.PDF SHALL BE REFERRED.





DETAIL-A(V-GROOVE DETAILS)
SCALE:NTS

DRILL CHART: TOP to BOTTOM

ALL UNITS ARE IN MILS

FIGURE	SIZE	TOLERANCE	PLATED	QTY
·	8.0	+3.0/-3.0	PLATED	3111
•	28.0	+3.0/-3.0	PLATED	64
•	36.0	+3.0/-3.0	PLATED	40
•	40.0	+2.0/-2.0	PLATED	33
•	40.0	+3.0/-3.0	PLATED	101
•	44.0	+2.0/-2.0	PLATED	18
■	62.0	+3.0/-3.0	PLATED	2
■	66.0	+3.0/-3.0	PLATED	4
■	78.0	+3.0/-3.0	PLATED	1
•	34.0	+1.0/-1.0	NON-PLATED	2
•	40.0	+3.0/-3.0	NON-PLATED	2
■	50.0	+3.0/-3.0	NON-PLATED	2
❖	64.0	+2.0/-2.0	NON-PLATED	1
❖	66.0	+3.0/-3.0	NON-PLATED	4
❖	92.0	+3.0/-3.0	NON-PLATED	2
❖	108.0	+3.0/-3.0	NON-PLATED	13
◈	124.0	+3.0/-3.0	NON-PLATED	2
◈	126.0	+3.0/-3.0	NON-PLATED	2
▬	52.0x24.0	+3.0/-3.0	PLATED	4
▬	52.0x26.0	+3.0/-3.0	PLATED	2
▬	64.0x32.0	+3.0/-3.0	PLATED	2
▬	80.0x40.0	+3.0/-3.0	PLATED	4
▮	82.0x34.0	+2.0/-2.0	PLATED	1

IMPEDANCE SPECIFICATIONS

SL#	TYPE	LAYER	TRACEWIDTH(Mils)	SPACING(Mils)	IMPEDANCE(Ohms)	REF LAYER
01	EDGE COUPLED STRIPLINE	L3,L8	3.2	7.5	100	L2/L4,L7/L9
02	EDGE COUPLED MICROSTRIP	L1,L10	4.25	7.15	100	L2, L9
03	EDGE COUPLED STRIPLINE	L3,L8	3.7	6	90	L2/L4,L7/L9
04	EDGE COUPLED MICROSTRIP	L1,L10	4.2	4.4	90	L2,L9
01	EDGE COUPLED STRIPLINE	L3,L8	4.2	4.3	80	L2/L4,L7/L9
02	EDGE COUPLED MICROSTRIP	L1,L10	6.02	6.8	80	L2,L9
03	EDGE COUPLED MICROSTRIP	L1,L10	4.1	5.75	120	L3
03	STRIPLINE	L3,L8	5.8	NA	40	L2/L4,L7/L9
04	MICROSTRIP	L1,L10	9.05	NA	40	L2,L9
04	STRIPLINE	L3,L8	3.6	NA	50	L2/L4,L7/L9
05	MICROSTRIP	L1,L10	5.8	NA	50	L2,L9

LAYER STACKUP

LAYER NAME	FINISHED Cu	DIELECTRIC THICKNESS [INCHES]
PRIMARY SIDE SILKSCREEN		
PRIMARY SIDE SOLDERMASK		
L01 — PRIMARY SIDE	1 oz.	0.0037
L02 — GROUND-PLANE-1	1 oz.	0.004
L03 — INNER-SIGNAL-1	1 oz.	0.0066
L04 — GROUND-PLANE-2	1 oz.	0.005
L05 — POWER-PLANE-1	1 oz.	0.009
L06 — POWER-PLANE-2	1 oz.	0.005
L07 — GROUND-PLANE-3	1 oz.	0.0066
L08 — INNER-SIGNAL-2	1 oz.	0.004
L09 — GROUND-PLANE-4	1 oz.	0.0037
L10 — SECONDARY SIDE	1 oz.	
SECONDARY SIDE SOLDERMASK		
SECONDARY SIDE SILKSCREEN		

SIGNATURES		DATE
LAYOUT BY	UD	030321
REVIEWED BY	ZA	030321
APPROVED BY	AMB	030321

TEXAS INSTRUMENTS

PROC101A

AM64x EVM BOARD

SIZE D | Rev A

SCALE:NONE | SHEET 1 OF 17